UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,035	07/03/2002	Gilbert Wolrich	10559-306US1	9914

20985 7590 05/04/2007

FISH & RICHARDSON, PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
05/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/070,035	WOLRICH ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5 and 7-22* is/are pending in the application.

4a) Of the above claim(s) *4 and 6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 7-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/23/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-3,5,7-22 remain for examination. Claims 4,6 have been canceled. Claims 1,10,16, 19 are rejected under 35 U.S.C. 101 the claimed invention is directed to non-statutory subject matter.

2. Claim 1 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 29 (claim 29 includes limitations of parent claim 23) of U.S. Patent No. 6,668,317. Although the conflicting claims are not identical, they are not patentably distinct from each other because although patented claim 29 did not recite the branch to the instruction at a specific address as claimed, patented Claim 29 did disclose the determination of witch thread to execute based on signal indicating the completion of requested (see patented claim 23, lines 10-14). It would have been recognizable to one of ordinary skill in the art that the determination of the thread could be a sequence of instructions with the leading instruction at a specific memory location or a predefined address. Although not specifically recited, one of ordinary skill in the art should be able to recognize the applicability of branching or pointing to the instruction at the specified address as claimed based on the execution of the thread determination.

3. Claims 1,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Cage (4,454,595) in view of Kiefer (6,223,208).

4. Claims 1,10,19, rejected under 35 U.S.C. 103(a) as being unpatentable over Aggarwal et al. (6,275,508) in view of Kiefer (6,223,208).

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa (5,724,563) in view of Kiefer (6,223,208).

6. As to the newly amended feature of causing to branch to another instruction at specified address, examiner holds that branch ahs to branch to an instruction at a predetermined address. Otherwise, branch would have no meaning.

8. The rejections have been maintained and incorporated by reference the last office action on 10/27/06.

9. The response filed by applicant on 02/06/07 has been fully considered but is not persuasive.

10. In the remarks, applicant argued that :

a) claim 1 has been amended to "device" instead of medium;

b) no branch can be found in claims 23,29;

c) no process of plurality of threads in Hasegawa;

d) Kiefer did not teach a configuration that includes a plurality of processors such as processor 200, nor state available to such plurality of processors;

e) Cage is not multithreaded;

f) Aggarwal did not teach multithreaded processor.

11. As to a) clam 1 also recites computer program product (see claim 1, line 1). It has the phrase of "cause" the execution of instruction stream to branch if a state is a specified value. It is read as intended result. Although claim recites the state indicating availability of resources to the plurality of micro engines, no substantial practical application can be found. Final result achieved which is useful, tangible, and concrete cannot be found. It is not specific because no definite final state can be found. It is not substantial because further actions by the micro engines being configured to process the plurality of threads is unclear. It is not credible because detailed components of the computer program product to impart the functionalities of the "micro engines" is not being recited.

12. Furthermore, It produces no tangible result because the computer program product residing on a computer readable storage device to cause to branch if a state is

at a specified value is an intended use, therefore an abstract idea. The evidence shows applicant is claiming "control logic" (see claim 1, line 8). Logic is an abstract idea.

13. Also, it is not concrete because it is not repeatable. No predictable result ahs been reflected into the claim that if the state is not a specified value. Therefore, unpredictable.

14. Similarly, clams 10, 19 also recited cause the processor to evaluate, perform, and configure to process the plurality of threads. No substantial practical application can be found. Although amended claim 19 recites causes a processor to perform a branch operation to cause an instruction stream of the processor to another instruction of the instruction at address specified in the branch instruction based on the specified value, it is an intended use. No clear predictable result can be found if the specified value is set or cleared.

15. As to claim 16, although claim 16 recites a register stack, an arithmetic logic unit coupled to program control store that stores a branch instruction that causes the micro engine to evaluate and perform the branch based on the specified value, no detail of the register stack no components of the arithmetic logic unit have been reflected into the claim. Therefore, the register stack and arithmetic logic unit are reads as general arrangement of the generic units. No substantial practical application can be found for performing the branch, nor the practical application be found for micro engines. Therefore, it is a non-statutory.

16. As to b) above, although patented claims 23, 29 did not recite the branch to the instruction at a specific address as claimed, patented claims 23,29 did disclose the determination of witch thread to execute based on signal indicating the completion of requested (see patented claim 23, lines 10-14). It would have been recognizable to one of ordinary skill in the art that the determination of the thread could be a sequence of instructions with the leading instruction at a specific memory location or a predefined

address. Although not specifically recited, one of ordinary skill in the art should be able to recognize the applicability of branching or pointing to the instruction at the specified address as claimed based on the execution of the thread determination, and a specified value could d be a specified signal.

17. As to c), Hasegawa did not specifically show threads as claimed. However, Kiefer taught the micro engine (see fig.2 [200]) having a control logic [context switching] and execution logic including the arithmetic unit [260]-[250] and general purpose unit [register set], and configured to process a plurality of threads (see the general purpose register and the execution of threads in col.8, lines 4-45). The reasons of obviousness were already provided in the paragraph 22 of the last office action on 12/22/06. Therefore, it will not be repeated herein.
As to d), Kiefer taught clearly that the number of the number and the type of the components in fig.1 (see col.7, lines 39-56; fig.1 Included CPU 100, and the CPU 100 included processor 200). Therefore, plurality of processors 200 were applicable as well.

18. As to e), Cage did not specifically show the micro engine having a control logic and execution logic including the arithmetic unit and general purpose unit, and configured to process a plurality of threads as claimed. However, Kiefer taught the micro engine (see fig.2 [200]) having a control logic [context switching] and execution logic including the arithmetic unit [260]-[250] and general purpose unit [register set], and configured to process a plurality of threads (see the general purpose register and the execution of threads in col.8, lines 4-45). The reasons of obviousness were already given in paragraph 13 of the last Office action. Therefore, not to be repeated herein.

19. As to f), see Page 8, Paragraph 18 in the last office action.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H PAN
PRIMARY EXAMINER
GROUP